Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	74	second adj DC with converter same (control$3 CPU $processor) same battery	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 17:21
S3	2	regulation adj sensing adj level	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 16:26
S4	355	307/82.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/30 16:27
S5	96	307/43-87.ccls. and converters same (CPU control$3 $processor) same battery	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/30 18:02
S6	11	307/43-87.ccls. and second adj DC adj3 converters same battery	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 17:21
S8	106	second adj DC adj3 converters same battery	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 17:38
S9	99	battery with DC adj2 DC adj2 converter and linear adj regulator	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 17:41
S10	9	battery with DC adj2 DC adj2 converter and linear adj regulator and 307/43-87.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 17:39

S11	90	S9 not S10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 17:41
S12	16	307/43-87.ccls. and battery same linear adj regulator	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/30 18:10
S13	1164	307/43-87.ccls. and battery same (regulator converter)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/30 18:16
S14	1083	307/43-87.ccls. and battery same (regulator converter) and (control$3 CPU $processor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/30 18:18
S15	256	307/43-87.ccls. and battery same DC adj DC same (regulator converter) and (control$3 CPU $processor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 12:25
S16	1389	DC with output with power same computer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 12:25
S17	328	DC with output with power same computer same battery	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 13:32
S18	421	DC with output with power same computer same battery	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 12:25

S19	229	DC with output with power same computer same battery and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 12:26
S20	138	DC with output with power with computer same battery and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 13:31
S22	1573	detect$3 with presen$3 with (source supply power) same compar$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 16:41
S23	831	detect$3 with presen$3 with source same compar$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 15:40
S24	405	detect$3 with presen$3 with source same compar$3 and @ay<"2001"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 15:41
S25	459	detect$3 with presen$3 with source same compar$3 and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 16:32
S26	1	S25 and 307/43-87.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 15:43
S27	6	S22 and 307/43-87.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 15:43

S28	35	detect$3 with presen$3 with source same compar$3 with voltage with output and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 16:33
S29	19	detect$3 with presen$3 with source same compar$3 with voltage with output same input and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 16:33
S30	15	detect$3 with presen$3 with source same compar$3 with voltage with output with input and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:21
S31	257	detect$3 with presen$3 with (source supply power) same compar$3 with voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 16:51
S32	99	detect$3 with presen$3 with (source supply power) same compar$3 with voltage not predetermined	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 16:54
S33	34	detect$3 with presen$3 with (source supply power) same compar$3 with voltage not (predetermined reference)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 16:54
S34	219	valid adj4 voltage same indicat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:21
S35	4	valid adj4 voltage same indicat$4 same steady adj state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:22

S36	64	output adj2 voltage same indicat$4 same steady adj state same (valid quality satisfactory)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:26
S37	10	output adj2 voltage with steady adj state same LED	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:29
S38	6911	voltage with steady adj state same (indicat$3 notif$5 signal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:29
S39	3946	voltage with steady adj state same (indicat$3 notif$5 signal) and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:39
S40	73	determine with voltage with steady adj state same (indicat$3 notif$5 signal) and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:43
S41	5	determine with voltage with steady adj state adj condition same (indicat$3 notif$5 signal) and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:44
S42	3	DC adj DC adj converter same sink adj transistor same source adj transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 18:26
S43	4789	DC adj DC adj converter same transistors	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 18:26

S44	1567	DC adj DC adj converter same transistors	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 18:26
S45	836	DC adj DC adj converter with transistors	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 18:26
S46	544	DC adj DC adj converter near9 transistors	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 18:27
S47	372	DC adj DC adj converter near9 transistors and @ay<"2002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 18:29
S49	506	power adj management and DC adj Dc adj converter same (control$3 $processor CPU)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 18:34
S50	2783	converter same transistors same (turn adj off disable deactivate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 18:35
S51	882	converter same transistors same (turn adj off disable deactivate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 18:38
S52	272	(turn adj off disable deactivate) with converter same transistors	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 18:39

S53	187	(turn adj off disable deactivate) with converter with transistors	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/01 18:39
S57	29430	steady adj state with (detect$3 reach$3 determin$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 10:16
S58	7	if with steady adj state with (detect$3 reach$3 determin$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 10:16
S59	110	steady adj state with (detect$3 reach$3 determin$3) same signal with sent	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 10:43
S60	40	steady adj state with (detect$3 reach$3 determin$3) same signal with sent same voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 10:47
S62	548	steady adj state with voltage with (detect$3 reach$3 determin$3) same (notif$6 indicat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/02 10:58